AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing Of Claims:

1-15. (Canceled).

16. (Currently Amended) A semiconductor system having a p-n junction, comprising:

a substrate having an edge region, which is made up of a first layer of a first conductivity type and a second layer of an opposite conductivity type, the second layer being made up of at least two sublayers, wherein:

the first sublayer has a first dopant concentration,

the second sublayer has a second dopant concentration that is lower than the first dopant concentration,

both sublayers together with the first layer form a p-n junction, the p-n junction of the first layer with the first sublayer being formed exclusively in an interior of the chip and the p-n junction between the first layer and the second sublayer being formed in the edge region of the chip,

the second layer includes a third sublayer having a third dopant concentration that is higher than the first dopant concentration and significantly higher than the second dopant concentration,

the third sublayer over a largest part of its cross-sectional area in the interior of the semiconductor system borders immediately on the first sublayer, while bordering on the second sublayer only in a comparatively narrow edge region of the cross-sectional area, wherein the first sublayer has a portion with a thickness greater than the second sublayer.

17. (Previously Presented) The semiconductor system of claim 16, wherein the sublayers of the semiconductor system at least one of touch in a central region of the semiconductor system, and overlap in regions.

18. (Previously Presented) The semiconductor system of claim 16, wherein a dopant concentration in each of the sublayers is higher than a dopant concentration in the sublayer forming the basic substrate.

19. (Previously Presented) The semiconductor system of claim 16, wherein in its central region the sublayers form a first p-n junction between a p+-doped and an n+-doped semiconductor substrate.

20. (Previously Presented) The semiconductor system of claim 16, wherein in its edge region the sublayers form a second p-n junction between a p+-doped and an n--doped semiconductor substrate.

21. (Previously Presented) The semiconductor system of claim 16, wherein it has in its edge region a wide, shallow sawing trench having a sawing width and a sawing depth, the sawing width being at least one of greater than 80 micrometers and 100 micrometers, and wherein a ratio of the sawing width to the sawing depth has a value greater than 3.

22. (Previously Presented) The semiconductor system of claim 16, wherein the sawing trench is completely filled with solder material so that the wall surfaces of a sawing trench are covered by solder material and are protected by this solder material.

23. (Previously Presented) The semiconductor system of claim 16, wherein the semiconductor system is part of a diode.

24. (Previously Presented) The semiconductor system of claim 16, wherein a breakdown voltage in the edge region of the semiconductor system is significantly greater than a breakdown voltage in a central region of the semiconductor system.

25. (Previously Presented) The semiconductor system of claim 24, wherein the breakdown voltage in the edge region is greater than the breakdown voltage approximately by a factor of 2 to 7.

26. (Previously Presented) The semiconductor system of claim 16, wherein a bulk resistance in a central region of the semiconductor system is lower than the bulk resistance in an edge region of the semiconductor.

27. (Currently Amended) A semiconductor system having a p-n junction, comprising:

a substrate having an edge region, which is made up of a first layer of a first conductivity type and a second layer of an opposite conductivity type, the second layer being made up of at least two sublayers, the first sublayer having a first dopant concentration and the second sublayer having a second dopant concentration that is lower than the first dopant concentration, both sublayers together with the first layer forming a p-n junction, the p-n junction of the first layer with the first sublayer of the second layer being formed exclusively in an interior of the chip and a p-n junction between the first layer and the second sublayer being formed in an edge region of the chip,

wherein a layer over a largest part of a cross-sectional area in the interior of the semiconductor system borders immediately on the first layer, while bordering on the second layer only in a comparatively narrow edge region of the cross-sectional area, wherein the first sublayer has a portion with a thickness greater than the second sublayer.

28. (Canceled).

29. (Currently Amended) A method for manufacturing a semiconductor system, comprising:

manufacturing a semiconductor substrate of a first conductivity type forming a first sublayer of the semiconductor system;

doping the first sublayer on both sides for forming two further sublayers of the same conductivity type as the first sublayer but with different degrees of doping so that the two sublayers touch or overlap at most in a central region of the semiconductor system;

producing a fourth sublayer of an opposite conductivity type by introducing a dopant into the sublayers and by increasing the dopant concentration of the sublayer;

covering outer surfaces of the sublayers with metallic contact layers;

wherein the semiconductor system has a p-n junction, including a substrate having an edge region, which is made up of the first layer of a first conductivity type and a second layer of an opposite conductivity type, the second layer being made up of at least two sublayers,

wherein:

the first sublayer has a first dopant concentration,

the second sublayer has a second dopant concentration that is lower than the first dopant concentration,

both sublayers together with the first layer form a p-n junction, the p-n junction of the first layer with the first sublayer being formed exclusively in an interior of the chip and the p-n junction between the first layer and the second sublayer being formed in the edge region of the chip,

the second layer includes a third sublayer having a third dopant concentration that is higher than the first dopant concentration and significantly higher than the second dopant concentration,

the third sublayer over a largest part of its cross-sectional area in the interior of the semiconductor system borders immediately on the first sublayer, while bordering on the second sublayer only in a comparatively narrow edge region of the cross-sectional area, wherein the first sublayer has a portion with a thickness greater than the second sublayer.

30. (Previously Presented) The semiconductor system of claim 16, wherein p-doped and n-doped layers are interchanged.